In re Patent Application of
BERTRAND ET AL.
Serial No. **10/813,564**
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In the Specification:

Please amend paragraph 28 on page 9 of the specification as follows:

[0028] According to the described mode of implementation (Figure 3) of the invention, the first negative feedback loop comprises an N-type transistor T22 and a P-type transistor T33. The source of the transistor T22 is connected to the point A1, the gate of transistor T22 is connected to the source of transistor T33 whose gate is connected to the output of the inverter I. The power supply potential VDD is applied to the drain of transistor T22, and the first ~~second~~ reference potential VREF 1 is applied to the drain of transistor T33.